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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,648	08/13/2001	Thomas H. Lee	035905/0104	6565

7590 06/25/2003

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EXAMINER	
WEISS, HOWARD	
ART UNIT	**PAPER NUMBER**
2814	13

DATE MAILED: 06/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Interview Summary	Application No.	Applicant(s)	
	09/927,648	LEE ET AL.	
	Examiner	Art Unit	
	Howard Weiss	2814	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Howard Weiss*.

(2) *Leon Radomsky*.

(3) *Dr. Thomas Lee*.

(4) *Liza Toth*.

Date of Interview: *24 June 2003*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *99,103,456,458-461,475 and 477*.

Identification of prior art discussed: *Watanabe, Kub*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *The substance of the interview followed that outlined in Form PTOL-413A as submitted by the Applicants and is attached*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

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Total # of Pages 8 (including this page)

TO:	PHONE #:	FAX #:
Examiner H. Weiss		**(703) 746-3889**

From :	**Leon Radomsky**
Date :	**June 23, 2003**
Client/Matter No :	**35905-0104**
User ID No :	**2350**

MESSAGE:

Dear Examiner Weiss,

As we discussed on the phone, enclosed is Form PTOL-413A and attachment listing the proposed topics for the telephone interview scheduled for 6/24 at 1:30 PM. Thank you for your consideration.

If there are any problems with this transmission or if you have not received all of the pages, please call 202.672.5340.

Operator:	Time Sent:	Return Original To: Leon Radomsky

Received from < 6391 > at 6/23/03 10:01:17 AM [Eastern Daylight Time]

PTOL-413A (03-03)
Approved for use through xx/xx/xxxx. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Applicant Initiated Interview Request Form

Application No.: 09/927648 First Named Applicant: Lee

Examiner: H. Weiss Art Unit: 2814 Status of Application: _____

Tentative Participants:

(1) Dr. THOMAS Lee (2) Leon RADOMSKY

(3) LIZA TOTH (4) _____

Proposed Date of Interview: 6/24/03 **Proposed Time:** 1:30 (AM/PM)

Type of Interview Requested:

(1) [X] Telephonic (2) [ ] Personal (3) [ ] Video Conference

Exhibit To Be Shown or Demonstrated: [ ] YES [X] NO

If yes, provide brief description: _____

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1)			[ ]	[ ]	[ ]
(2)			[ ]	[ ]	[ ]
(3)			[ ]	[ ]	[ ]
(4)			[ ]	[ ]	[ ]

[X] Continuation Sheet Attached

Brief Description of Arguments to be Presented:

Please see ATTACHED

An interview was conducted on the above-identified application on _____.

NOTE:

This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP § 713.01).

This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible.

(Applicant/Applicant's Representative Signature) (Examiner/SPE Signature)

Atty. Dkt. No. 035905-0104

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Thomas H. LEE et al.

Title: DENSE ARRAYS AND CHARGE STORAGE DEVICES, AND METHODS FOR MAKING SAME

Appl. No.: 09/927,648

Filing Date: 08/13/2001

Examiner: H Weiss

Art Unit: 2814

PROPOSED TOPICS FOR TELEPHONE INTERVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

I. **Proposed new title:**

"A monolithic three dimensional array of charge storage devices containing a planarized surface."

II. **Proposed claim amendments:**

101. The semiconductor device of claim 99, wherein at least one surface between two successive device levels of the array is planarized by chemical mechanical polishing.

III. Proposed new claims:

483. The semiconductor device of claim 99, wherein the charge storage devices comprise non-volatile charge storage devices.

484. The semiconductor device of claim 99, wherein the array of charge storage devices is formed in a plurality of amorphous or polycrystalline semiconductor layers over the monocrystalline semiconductor substrate.

485. The semiconductor device of claim 484, wherein the plurality of amorphous or polycrystalline semiconductor layers comprise a plurality of amorphous or polycrystalline silicon layers.

486. The semiconductor device of claim 99, wherein the driver circuitry is formed in the substrate at least in part under the array.

487. The semiconductor device of claim 99, wherein the driver circuitry is formed within the array.

488. The semiconductor device of claim 99, wherein the driver circuitry is formed above the array.

489. The semiconductor device of claim 456, wherein the charge storage devices comprise non-volatile charge storage devices.

490. The semiconductor device of claim 456, wherein the array of charge storage devices is formed in a plurality of amorphous or polycrystalline semiconductor layers located over a monocrystalline semiconductor substrate.

491. The semiconductor device of claim 475, wherein the charge storage devices comprise non-volatile charge storage devices.

492. The semiconductor device of claim 475, wherein the array of charge storage devices is formed in a plurality of amorphous or polycrystalline semiconductor layers located over a monocrystalline semiconductor substrate.

493. The semiconductor device of claim 475, wherein the charge storage devices of the array comprise pillar TFT EEPROMs.

494. The semiconductor device of claim 475, wherein the charge storage devices of the array comprise pillar diodes with a charge storage region.

495. The semiconductor device of claim 475, wherein the charge storage devices of the array comprise self aligned TFT EEPROMs.

496. The semiconductor device of claim 475, wherein the charge storage devices of the array comprise rail stack TFT EEPROMs.

497. The semiconductor device of claim 496, wherein:

the array contains four or more device levels; and

the surface of an interlayer insulating layer located between two levels is planarized by chemical mechanical polishing.

IV. Arguments

1. Claim 456

- Watanabe does not teach a planarization step for any layer of the array by any planarization method.
  - The terms "planar member" in Watanabe refer to as-deposited conductive layers, such as word lines or bit lines (see col. 2, lines 67-68, col. 3, lines 60-61, and col. 4, lines 67-68). These conductive layers are not planarized by a planarization step.
- Claim 456 recites that at least one surface is planarized by CMP. Surfaces of a layer planarized by CMP have a high degree of planarity, even when the layer is deposited over non-uniform device features.
- The claimed surface would have a different structure than a surface of the as-deposited "planar members" of Watanabe because of the higher planarity of the claimed surface.
  - The surfaces of the "planar members" or conductive layers of Watanabe would have a lower degree of planarity than the claimed surface because the layers of Watanabe are deposited over non-planar device features in lower levels and/or on the substrate.
- MPEP 2125 states that proportions or features in prior art drawings are not evidence of actual proportions unless the prior art expressly states that drawings are to scale.
  - Just because the figures of Watanabe show straight horizontal lines does not mean that the actual layers of Watanabe are highly planar.
- 3D array of Figure 6 of Watanabe is not monolithic because "planar members" are bonded together (col. 6, lines 6-8).
- Applicants request rejoinder of claim 467 upon allowance of claim 456.

2. Claim 475

- Kub teaches that when two wafers are bonded together, the wafer surfaces being bonded should be polished by CMP to improve wafer bonding.
- Claim 475 recites a monolithic 3D array. A monolithic 3D array by definition does not use wafer bonding to bond separately formed device levels together, as defined on page 19, lines 10-14 of the present specification:

> The term "monolithic" means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

- There is no motivation to import the CMP method / surfaces of Kub into a monolithic 3D array because Kub teaches that CMP improves wafer bonding, while a monolithic 3D array does not include bonded wafers.

3. Claim 99

- Claim 99 recites that the devices are formed in an amorphous or polycrystalline semiconductor layer.
- Watanabe does not state that the silicon layers of the array are either amorphous or polycrystalline.
- Watanabe teaches that the silicon layers are formed by vapor phase epitaxial method (col. 3, line 29-34), which implies that the silicon layers could be single crystal silicon layers.

4. **Claims 103, 458-461 and 477**

- Watanabe teaches a broad genus of devices ("any type of memory device", col. 2, lines 52-53). However, Watanabe does not teach or suggest the species of devices recited in claims 103, 458-461 and 477.
- In a case where the prior art teaches a broad genus, the prior art also has to provide motivation to select the claimed species from the broad genus (see MPEP 2144.08).
- Watanabe provides no such motivation. For example, Watanabe does not teach or suggest to make rail stack TFT EEPROMs as recited in claim 461.

V. **IDS**

Applicants respectfully request that the examiner acknowledge IDS's filed 11/27/01 and 6/11/02 in the next Office Action.

Respectfully submitted,

Date 6/23/03

By _____
Leon Radomsky
Attorney for Applicant
Registration No. 43,445

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